

A NEW METHOD FOR MMIC PARAMETRIC YIELD REALISTIC EVALUATIONS

Ezio Maria Bastida and Maurizio Pagani

Alcatel Telettra
Via Trento 30, 20059 Vimercate (Mi)
Italy

ABSTRACT

The paper first reports some new results recently obtained at Alcatel-Telettra on the functional yield calculation for large MMICs. The parametric yield evaluation tools usually available for foundry customers are then critically discussed. Subsequently, a very wide and self consistent data base on the MMIC MESFET statistical behaviour is described. Finally, a semiempirical MESFET model is analyzed, which allows accurate forecasts of the MMIC parametric yield by using such data base.

Keywords: MMIC yield, parametric yield, yield driven design.

1. INTRODUCTION

An impressive research effort has been recently dedicated [1] to the problems posed by the high yield and quality MMIC producibility. In spite of this effort and of the fact that the overall circuit cost increases as the ratio of chip area and circuit yield, it is still very difficult to obtain accurate evaluations of the overall yield of a given circuit topology especially when using the information usually available from foundries [2]. Moreover, detailed and reliable data on process related MMIC yields are usually not available in the open literature.

This paper describes the results obtained at Alcatel-Telettra as a consequence of a systematic approach aimed at fully overcoming these problems. The research program relevant to such an effort was previously reported [3] in a paper including a detailed analysis of the different factors (line, functional, parametric, dicing and assembling) determining the overall MMIC yield. The special importance of the functional and parametric yield data were subsequently outlined in a general paper [4] dedicated to the efficient development of mass producible MMICs.

The present work adds to the consideration previously developed on the functional yield evaluation further results recently obtained in the case of complex MMICs. A critical examination is then performed of the available parametric yield evaluation criteria. Particular attention will be dedicated to the MMIC development by using foundry services. The results will be then reported and discussed of a very wide and selfconsistent experimental data base (including both scattering and equivalent circuit parameters) on the MMIC MESFET statistical behaviour.

A simple and flexible MESFET statistical model is then described which by making use of these data permits very accurate parametric yield forecasts to be obtained. The model is physics based type but includes a semiempirical allignment of the relevant parameters and seems particularly suitable for yield driven design centering procedures. It was previously [4] defined around a fixed bias condition [$V_{ds}=5V$ $V_{gs}=-1V$ (corresponding to $I_{ds}=0.5I_{dss}$)] but its practical extension to a different bias condition will be here considered.

Finally, the validity of the proposed model will be demonstrated by making reference to the calculated and the experimental parametric yield of some MMIC circuits we produce from over two years.

2. FUNCTIONAL YIELD EVALUATION FOR COMPLEX CIRCUITS

Following our definition [4] the functional or d.c. yield represents the fraction of on wafer chips where all the single circuit elements pass an ideal full d.c. test.

This evaluation system includes the visual inspection results and corresponds to a careful consideration of the components d.c. behaviour. For example, a spiral inductor having short circuited tracks is discarded because it has not the right d.c. resistance.

The simplest way to evaluate the MMIC functional yield is to define a mean value for each circuit element [5]. However, as outlined in [2,4] this criterium suffers from the fact that the d.c. yield depends from the single element size.

In order to overcome this limitation, on the basis of our MMIC design and development experience, mainly focused on the production of mass producible monolithic circuits with low costs, we derived the functional yield calculation rules reported in ref.4. These rules, for this type of circuits, allowed to obtain an excellent agreement of predicted with measured functional yield values.

However, with the growing number of MMICs produced in Alcatel-Telettra, the need of studying and developing complex circuits for special applications [2] has involved some production experiments on this type of circuits [6,7].

The results of such experiments have put into evidence that the calculation system we described elsewhere [2,4] for high yield mass producible MMICs, gives, for very complex circuit topologies, underestimated functional yield evaluations.

In order to correct this error, while maintaining the forecasting accuracy of the previous functional yield calculation method in the case of mass producible circuits, it was introduced the so called defect density concept [2] functional yield calculation system.

Because of the fact that $(1-x)^n$ can be approximated, for small nx values, with $(1-nx)$ the old and the new method give results practically identical in the case of mass producible high yield circuits.

Figure 1 summarizes the functional yield results obtained by the defect density approach in the cases of FET devices, via holes, air bridges, MIM capacitors and thin film resistors.

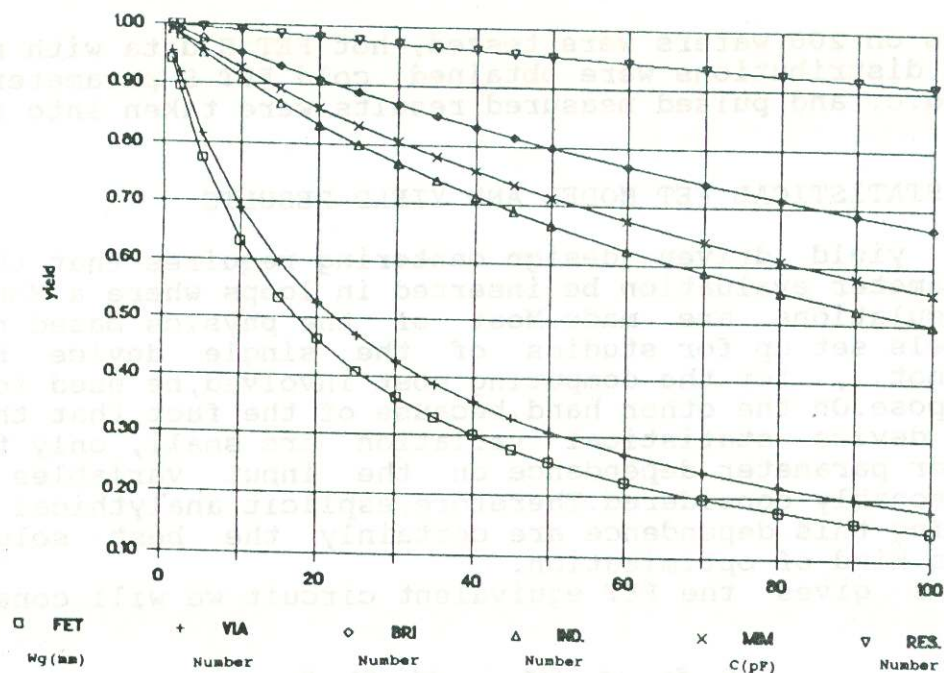


Figure 1: Defect density results for complex MMICs.

3. PARAMETRIC MMIC YIELD EVALUATIONS

The MMIC parametric yield, for given r.f. performance acceptance limits, is usually estimated with statistical tools (e.g. Monte Carlo routines, easily available in commercial circuit simulation CAD packages) on the basis of the single component process related performance fluctuations. Almost all the available GaAs foundries give this information in terms of mean value and standard deviation of the single device equivalent circuit parameters (ECPs) on the same wafer and from wafer to wafer.

The most important devices in determining the parametric yield are, as well known, the active ones. The relevant ECPs are often extracted from hot device S parameter measurements with procedures which suffer from the numerical optimization method employed and lead to parameter values not very correct from a physical point of view (i.e. far from those obtained by direct parameter measurements with other methods or from trustworthy calculations).

For this reason, it is not surprising that the parametric yield evaluations based on these data are far from the experimental values even when (quite a rare case) the ECP correlation matrix is available.

Moreover, it has been demonstrated that if the scattering parameter data base is not sufficiently large or shows bimodal distributions the deduced ECP statistics may fail in reconstructing that of the original S parameters.

This work shows how parametric yield evaluations much more close to the experimental results can be obtained. This is achieved by using a physics based device model which allows a very accurate representation of both ECP and S parameters statistical data base we collected, starting from a set of really uncorrelated process related variables, which can be easily measured or evaluated by MMIC manufacturers.

The used data base was constructed by making a great quantity of experimental measurements for each device bias point: 2300

FETs on 200 wafers were tested, hot FET S data with no bimodal distributions were obtained, cold FET S parameter as well as d.c. and pulsed measured results were taken into account.

4. STATISTICAL FET MODEL AND YIELD RESULTS

The yield driven design centering requires that the device parameter evaluation be inserted in loops where a Monte Carlo calculations are made. Most of the physics based numerical models set up for studies of the single device behaviour cannot, for the computing cost involved, be used for such a purpose. On the other hand, because of the fact that the device to device statistical variation are small, only the first order parameter dependence on the input variables can be reasonably considered. Therefore, explicit analytical formulas giving this dependence are certainly the best solution to this kind of optimization.

Fig.2 gives the FET equivalent circuit we will consider and

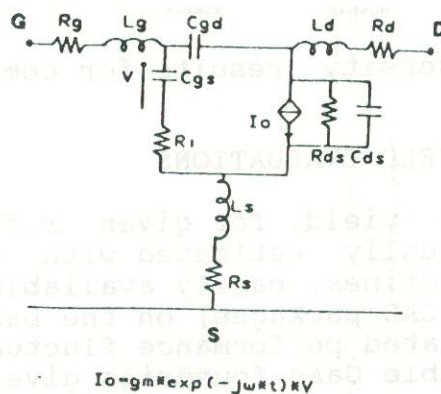


Figure 2: Equivalent circuit for the FET devices.

fig. 3 depicts the origin of the input process related

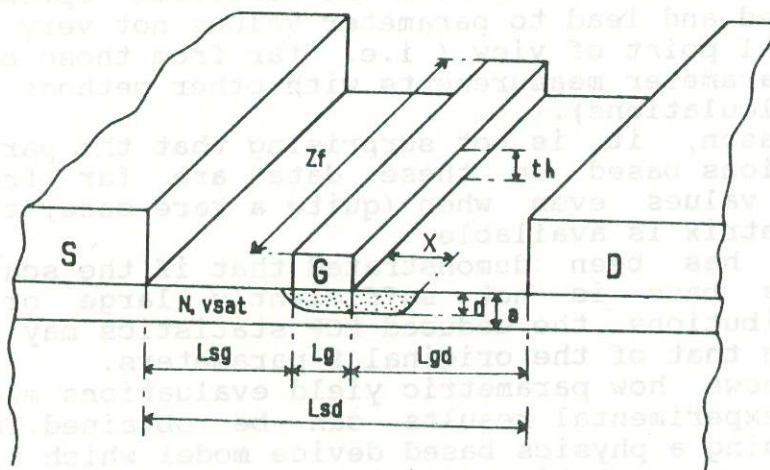


Figure 3: Origin of the input statistical data.

statistical data we consider. Table 1 gives the mean values

PARAMETER	MEAN VALUE	STAND.DEV.	UNITS
Peak doping density N	2.55E17	0.063E17	cm ⁻³
Active layer thickness a	0.148	0.0017	um
Gate length Lg	0.5	0.05	um
Gate to source distance Lsg	1	0.18	um
Saturated drift velocity vsat	0.9E7	0.047E7	cm/s
Builtin voltage Vbo	0.75	0.038	V

Table 1. Process related fluctuating parameters.

and the standard deviations of the used input data. The statistical FET model uses explicit relationships of such data and is based on a combination of the Ladbroke [8] physical model and of the Fukui [9] semiempirical formulas. Moreover, it makes use of empirical parameters for centering the mean values of the calculated parameters over the experimental one. Ref.[4] gives all the considered analytical relationships, which are here omitted for brevity. The model was first set up for a fixed bias condition ($V_{ds}=5V$, $V_{gs}=-1V$) and has the property of allowing a careful description of the distribution of each device ECP. At the time of writing we have verified and extended its validity to two additional bias points: ($V_{ds}=4V$, $V_{gs}=-1V$) and ($V_{ds}=3V$, $V_{gs}=-1V$). Further work is now in progress. Figures 4 and 5

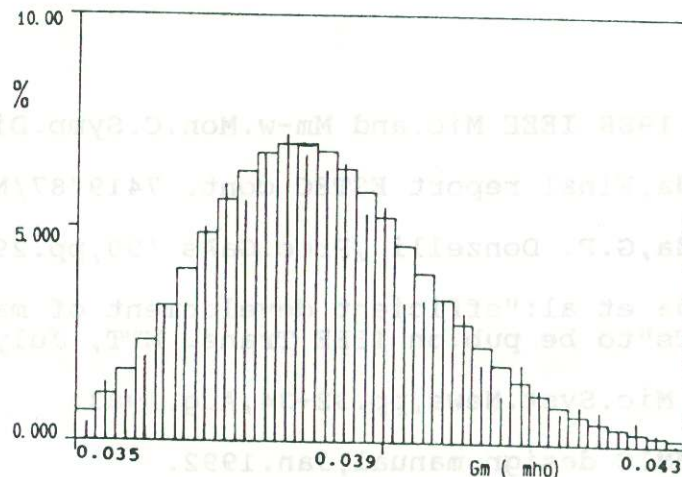


Figure 4: Experimental (vertical segments) and modeled (rectangles) gm values for $V_{ds}=4V$, $V_{gs}=-1V$.

give some examples of the correspondence of the experimental parameter histograms (vertical segments) to those deduced from the model. More details about the data base will be reported and analyzed during the oral presentation.

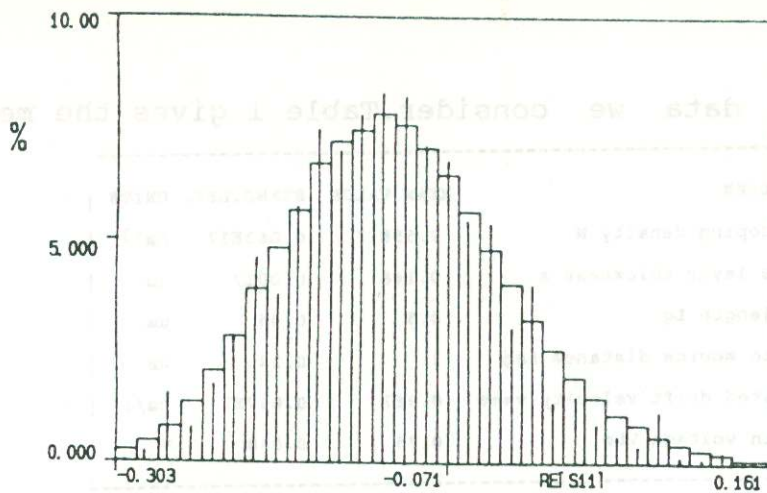


Figure 5: Experimental (vertical segments) and modeled (rectangles) $\text{Re}(S_{11})$ values for $V_{ds}=4V$, $V_{gs}=-1V$ at the operating frequency of 10GHz.

This approach has permitted us of evaluating, with a maximum error of 2% (instead of 30%-70%), the parametric circuit yield of three MMICs we have produced for over two years.

5. CONCLUSIONS

Results for calculating the functional yield of complex MMICs have been reported. The available parametric yield evaluation tools have been examined and discussed. A new method for obtaining accurate MMIC parametric yield forecasts has been described. Experimental evidence of this accuracy has been given.

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